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Department of Electronics & communication Engineering

Question Bank

Unit I

Q1) i) State Einstein's relation. Determine the concentration of free electrons &holes in a Ge sample at 300k which has a concentration of donor atoms equal to 4×10^{14} atoms/cm^3 & acceptor atoms equal to5×10^{14} atoms/cm^3. Is this P or N type Ge.

ii) Repeat above for a equal donor &accepter concentration of 10^14 atoms/cm^3.

Q2) A 230v, 60Hz voltage is applied to a primary of 10:1 stepdown centre tap transformer in full wave rectifier having load of 250Ω. If diode &sec coil resistance together is 100Ω.

Determine:

i)D.C output voltage.

ii)Rectification efficiency.

iii)PIV

iv)Output Frequency.

Q3) State Mass Action. Find out the conductivity of silicon for

1) In intrinsic condition at room temp.

2) With Donar impurity of 1 in 10^8.

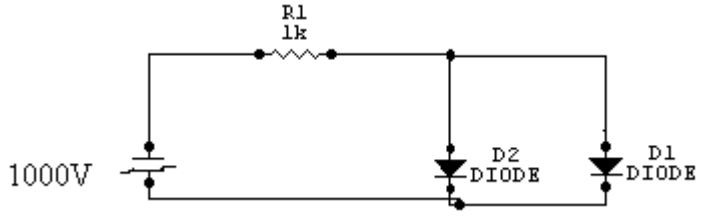
3) With Acceptor impurity of 1 in 5×10^7

4) With both the above impurity added simultaneously.

Given that ni for silicon at 300° is $1.5\times10^{10}/cm^3$, μn=1300cm^2/ V-S, Number of Si atoms per $cm^3=5\times10^{22}$.

Q4)Discuss briefly: Storage capacitance of p-n junction diode.

Each diode shown in fig.1 is modeled by a piece wise linear characteristics. Diode D1 is a Ge diode with Rf=20Ω and Vr=0.2V whereas diode D2 is a Ge diode with Rf=15Ω and Vf=0.6. Find out the diode currents.



Q5) For a full wave rectifier circuits, With a capacitor input filter, Derive the expression for ripple factor? A FWR circuit uses a capacitor filter with 50µf capacitor and provides a load currents of 200mA at 8% ripple, Find out the d.c voltage across the load?

Q6) State Mass Action law? A bar of intrinsic Si having a cross sectional area of $2.5\times10^{-4}m^2$ electron concentration of $1.5\times10^{16}/m^3$.What is the length of the bar in order to have a current of 1.2 miliamp, when 9V are applied across its ends?

(Assume: $Mp=0.05m^2$/V-sec ,$Mn=0.14m^2$/V-sec,$q=1.6\times10^{-19c}$)

Q7) A full wave rectifier uses Si diodes with a forward resistance of 20 ohm each.

A DC Voltmeter connected across the load of 1kohm reads 55.4 volts.

Calculate:

1) R.M.S. Value of load current.
2) Ripple Factor.
3) D.C. power given to load.

4) Transformer secondary ratings.

Q8) Explain:

1) PIN Diode.

2) Schottky Diode

Q9) A Sample of Germanium at 300K has a concentration of donor atoms equal to 2×10^{14} atoms/cm^3 and a concentration of acceptor atoms equal to 7×10^{13} atoms/cm^3.Find the concentration of free electrons & holes and state the type of semiconductor (N or P) hi=2.5×10^{13} /cm^3 at 300K.

Q10)) Define drift and diffusion current? A specimen of “Si”is 0.3mm long and has a C/S of 0.3mm*0.3mm,2V is applied across the bar which results in a current of 8mA.Assuming the current is due to electrons calculate:

1) Concentration of free electrons.

2) Drift Velocity.

Given at 300K, μ_n=1300 cm^2/V-sec.

QUESTION BANK OF SD&C

UNIT-II

1) Draw the circuit diagram for voltage divider biasing and explain the working.Write the equation for calculating Icq and VcEq.Derive the equation for stability factor.

2) For the voltage divider biasing circuit as shown in the figure (1) with Si transistor having β = 50, S$\leq$3, & Q_{pt} [11.5V, 1.5mA]. Calculate the values of R_1, R_2 & R_E. Assum R_c = 5kΩ and V_{CC} = 20V. **(10)**

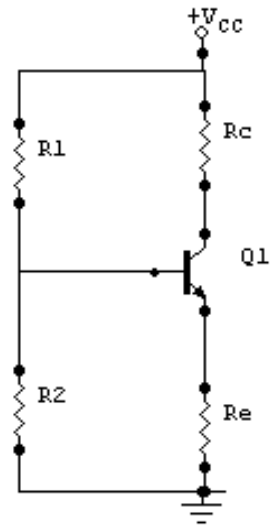
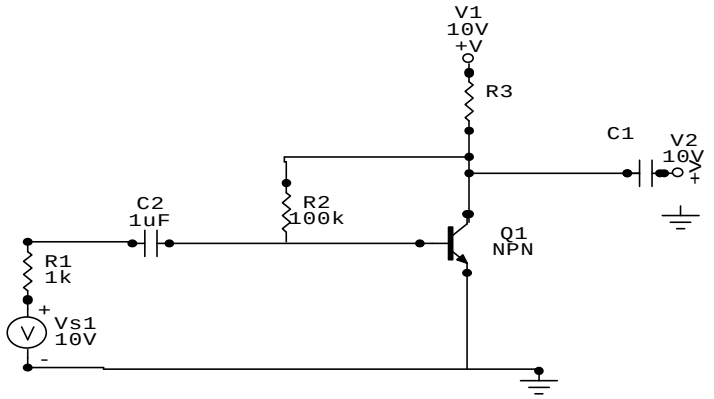


Fig.1

3) For a single stage amplifier in fig. Find out.

1) A_{vs} =V_o/V_s 2) A_{is} =I_l/I_s 3) R_i 4)R_0

Used transistor have h_{ie}=1K, h_{fe}=55.



4) For a C.C transistor amplifier supplied by a voltage source with internal resistance of 600ohm the load resistance is 1kohm.Find out-1) A_i 2)R_I 3)A_v 4) A_{vs} 5) R_0 using exact Analysis. The CE h Parameters are h_{fe}=60,hie=1.2K,hre=$2*10^{-4}$, hoe=25mA/V.

5) What is Thermal runaway? Derive the expression for stability factor $S=I_c/I_0$ for a potential-divider bias Network?

6) Draw the circuit diagram of collector to base bias biasing method. Derive the equation for Q-point and stability factor.

7) Explain: 1) Millers Theorem

2)Bootstrapped amplifier.

8) Draw the 'h' parameter equivalent circuit for a single stage CE amplifer and derive expression for Av, Ai and Ri.

of this circuit

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9) Write note on the following:

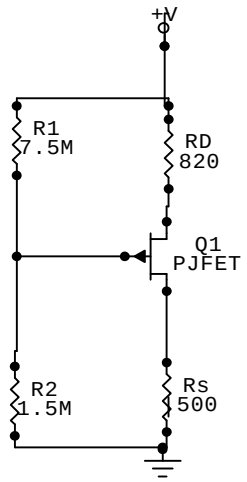
i. Temperature compensation methods.

Ii Thurmal Runaway in Transistors.

10) Draw darlington pair amplifer circuits. What is the significance of darlington circuits? Give advantages & disadvantages?

Unit –III

Q1) For a p- channel JFET Bias circuits in fig 3, if Vdd=-18V, Rf=7.5MΩ, R1=1.5MΩ, R2=1.5MΩ, Rd=820Ω,Rs=500Ω IDSS=18mA, Vp=+5V Graphically determine the quiescent value of Id and Vgs and use it to determine value of VDS?

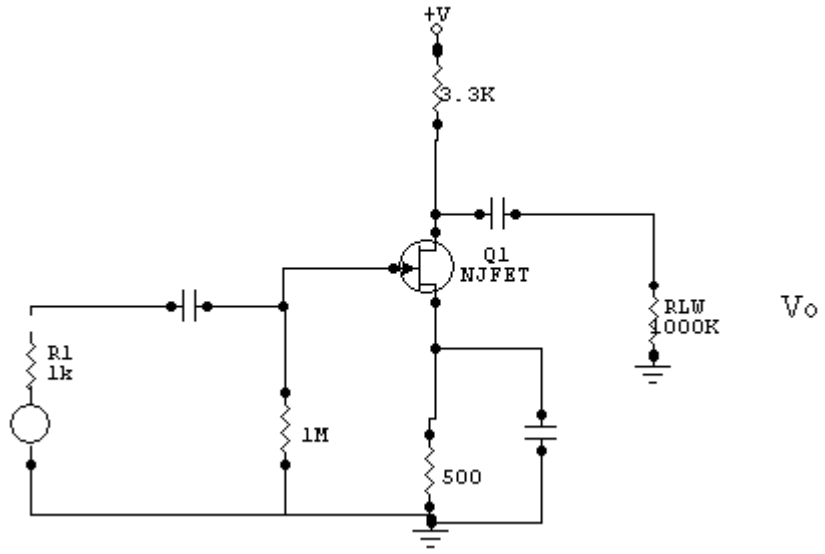


Q2) Write notes (i) Parameters of JFET.

(ii) Drain characteristics of n-channel JFET.

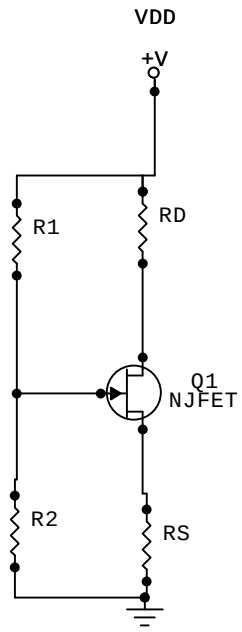
Q3) For the JFET-Cs amplifier shown in fig .4 find out of values of

i) Avs=V0/Vs ii) R1' iii) Ro' if gm =2ms and rd 50kΩ



Q4) For n-channel JFET Bias circuits in fig 3 if

Vdd=16V, Ri=2.12MΩ,R2=270kΩ,Rd=2.4k,Rs=1.51 ,Idss=8mA,Vp=-4V. Graphically find out the quiescent value of Id and Vgs, and use it to determine value of Vds?

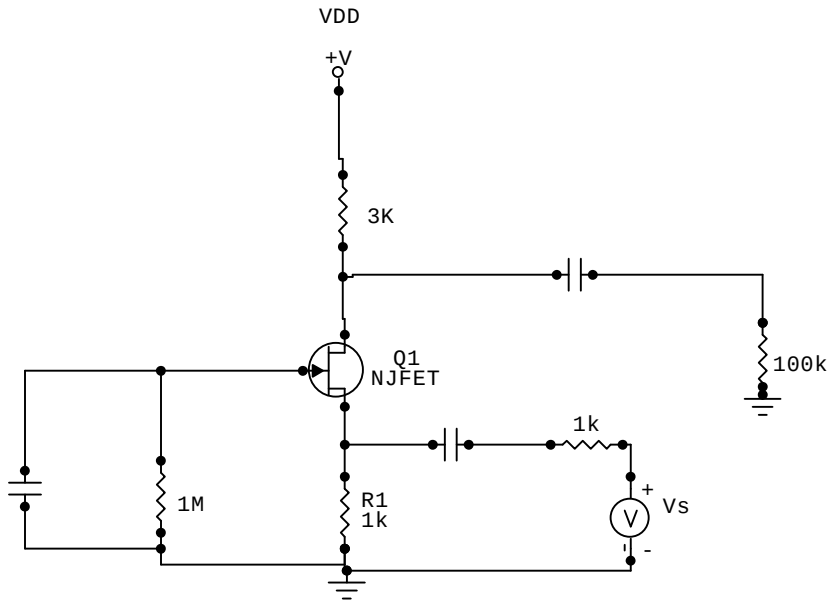


Q5) Write-

i) Drain characteristics of JFET.
ii) Compare BJT with FET ?

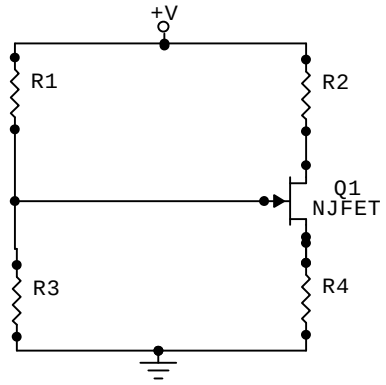
Q6)For the JFET amplifer in fig 4 find out

1) AVS=Vo/Vs 2) Ri' 3)Ro'
If gm=2m ,rd=40Ω



Q7) For a voltage divider bias circuit in fig. 3 calculate the values of I_{Dq}, V_{Dsq}, V_{Gsq} using graphical Approach?

Take R_1=20k,R_2=10k,$R_{D=}$1.5 k,R_S=1.5 k,V_{DD} =12 volts,I_{DSS} $V_{P=}$-4 V.Also find out the values of g_m?



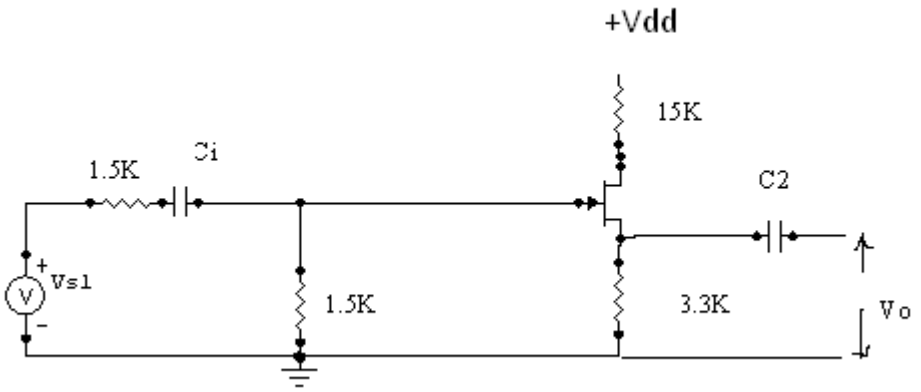
Q8) The amplifier shown in fig 4 uses n-channel JFET with g_m=5 m mho and r_d=18 kilo ohm. Calculate:

1) $A_{Vs}=V_0/V_s$

2) $A_v=V_0/ V_G$

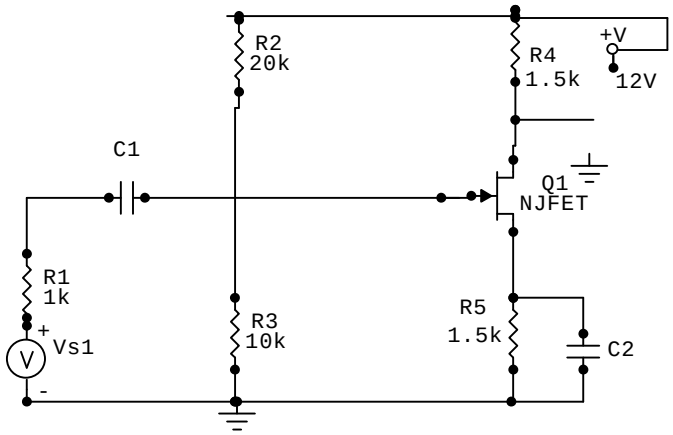
3) R_i

4) R_0 & $R'_{0.}$



Q9) Explain the output (drain) characteristics of p-channel JFET, clearly showing the cutoff, saturation and ohmic region ? Also define the parameters of JFET?

Q10) For the JFET amplifier in fig.4 find out Q points using analytical approach. Take I_{DSS}=12mA,V_p=-4V.



UNIT IV

1)With the help of constructional diagram and output (Drain) characteristics explain the operation of n – Enhancement MOSFET?

2)Write short notes on:

i) Power MOSFET ii) Body effect in MOSFETs.

3) For the bias network shown in the figure (1) Calculate V_{GSq}, I_{Dq} and V_{DSq} if V_{DD} = 12V, R_1 = 2.2MΩ, R_2 = 1.5Ω, R_D = 22K, R_S = 12k, V_{TN} = 1V, k_n = 500 × 10-6 A/V^2. Use

equation $I_D = \frac{k_n}{2}[V_{gs} - V_{TN}]^2$.

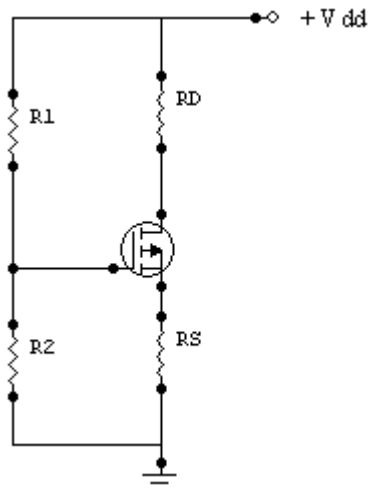


Figure (1)

4)With the help of constructional diagram and output (Drain) characteristics explain the operation of n – depletion MOSFET?

5)For the bias network shown in the figure (2) Calculate V_{GSq}, I_{Dq} and V_{DSq} V_{DD} = 10V, R_1 = 2MΩ, R_D = 20K, V_{TN} = 1V, k_n = 500 × 10-6 A/V. Use equation

$I_D = \frac{k_n}{2}[V_{gs} - V_{TN}]^2$.

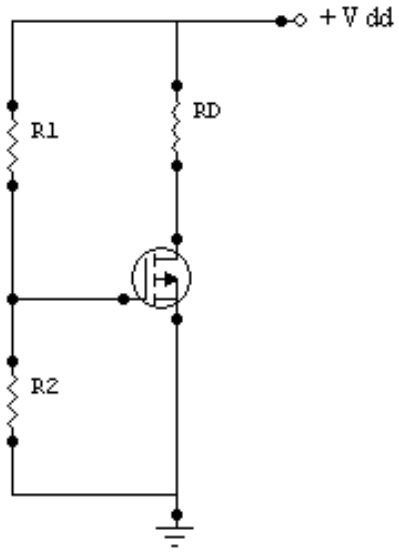


Figure (2)

6)Write notes on:

1. VMOS
2. Body effect in MOSFETs.

7)With the help of constructional diagram and output (Drain) characteristics, explain the operation of n – channel depletion MOSFET?

8) Related to CMOS Inverter, explain

i. Static Characteristics
ii. Noise Margin

9)Explain the working of EMOSFET. Draw the construction of EMOSFET. Draw the V-I characteristics for it and explain ohmic and saturation region.

10)Draw the circuit diagram of CMOS invertor and explain the working of it. Define the noise margin and threshold voltage.

UNIT –V

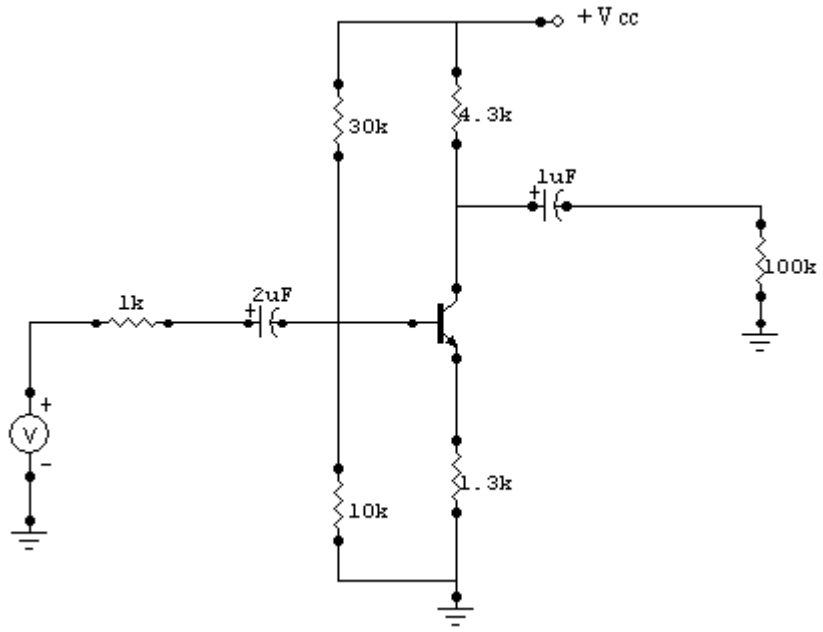
Q1)Explain the concept of Gain bandwidth in an amplifier? For 3 stages cascaded amplifier, the individual value of f_L and f_H is 2 kHz & 5 MHz respectively. Find out the bandwidth of complete composite amplifier?

Q2)Write note on the following:

i. Frequency Response of an amplifier.
ii. Effect of coupling and By- pass capacitors on frequency response.

Q3)Derive the equations of f_L and f_H for an amplifier obtained using square wave testing method?

4)For a CE amplifier in figure(1) determine the value of lower cut-off frequency. Take h_{fe} = 100, h_{ie} = 2kΩ, r = 50kΩ for the BJT.



Figure(1)

5)Why square wave is preferred for the testing purpose of an amplifier? The following measurements are taken while testing an amplifier using square wave input waveform:

i. For a square wave frequency of 5 kHz, the rise – time of output waveform is 20μsec.
ii. For a square wave input frequency of 100 Hx, there is a stage of 1 volt in 2.5 volts amplitude, observe on CRO.

Determine the bandwidth of amplifier under test?

6)For nth identical stages cascaded amplifier, derive the equation of lower and upper cut- off frequencies for complete amplifier?

7)Derive the equation for lower cut-off and higher cut-off frequency obtained using square wave testing method for an amplifier?

8) For a N stage cascade amplifier derive the expression for higher overall cutoff frequency for this amplifier?For a 4stage cascade amplifier the values of overall cut off freq for lower it is 200Hz and for higher it is 40kHz.Calculate the cutoff frequencies for individual amplifier.

9)Explain the significance of gain bandwidth product in amplifier? In 4 stages cascaded amplifier, the individual lower and higher cut-off frequency of amplifier is 1 KHz and 10 MHz respectively. Find the bandwidth of cascaded amplifier?

10)What is the square wave testing ? Explain how it is used for defining frequency response of amplifier. Define rise time and tilt or sag. If three identical cascade stage has overall 3Db f_H=25 kHz and f_L=20Hz.find f_L and f_H for each stage.