SHRI SANT GADGE BABA COLLEGE OF ENGINEERING & TECHONOLOGY, BHUSAWAL
Department of Electronics & Communication Engineering.

VLSI DESIGN (ELECTIVE-I) B.E (E&C)
Question Bank
Unit – I

NOV-DEC 2008

1) If A & B are two unsigned variables, with A = 1100 and B = 1001, find the values of following expressions. **(10)**
   i. (A and B)
   ii. (A ^ B)
   iii. !(B)
   iv. As/r3
   v. (A&&B)
2) Compare between VHDL and Verilog. **(10)**
3) Explain different operators of VHDL and Verilog. **(10)**

MAY-JUNE 2009

4) Write a VHDL and Verilog description for a half adder using behavioural and dataflow style of modeling. **(10)**
5) Compare between VHDL and Verilog. **(10)**
6) Discuss VHDL data types in detail. **(10)**

APRIL/MAY 2010

7) Explain structure of VHDL & Verilog with reference to
   i) Operators
   ii) Data types
   iii) Ease of learning
   iv) Library & packages
   v) Procedure & tasks **(10)**
8) List & Explain different styles of description **(10)**
9) Explain structure of VHDL & Verilog **(10)**

NOV/DEC 2010

10) If A and B are two unsigned variable with A=0110 and B=1010 find the values of Following expression:
    i) (A and B)
    ii) (A ^ B)
    iii) !(A)
    iv) A SRA 1
    v) (A && B) **(10)**
11) Explain different datatypes of Verilog **(10)**
12) Explain structure of VHDL and Verilog **(10)**

APRIL /MAY 2011

13) Determine whether the following statements are VHDL, Verilog or can be both **(10)**
 i) port (input 1: std_logic; output 2: std_logic);
 ii) y= s ^ sel ;
 iii) module vhdl ⊥ (I_1, I_2, O_1, O_2);
 iv) process Verilog (a,b,c)
 v) begin

14) List and explain different styles of descriptions. **(10)**
15) Explain different operators of VHDL. **(10)**

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16) Write history of VHDL & Verilog. **(10)**
17) Write Structural and data flow description for half adder. **(10)**
18) Explain simulation and synthesis with flow. **(10)**

APRIL /MAY 2012

19) Explain data types in verilog with suitable example .Explain importance of std_logic data type in VHDL. **(10)**
20) Write structural description of full adder (1 bit) in VHDL and verilog.The code must include the description for components used. **(10)**
21) If A and B are two unsigned variables ,A=1100 & B=1001 find the following . **(10)**
 i) A AND B ii) A ^ B iii) A NOR B iv) A & B v) A&&B vi) !B
 vii) ~ | (A) viii) A slr 3 ix) A>>1 x) B ror 2

NOVEMBER/DECEMBER 2012

22) Explain in detail Arithmetic operators in VHDL and Verilog. **(10)**
23) Explain structure of VHDL and Verilog Module. **(10)**
24) Explain different data types in VHDL. **(10)**

APRIL /MAY 2013

25) List and explain different styles of description. **(10)**
26) Explain in detail shift and rotate operators in VHDL and Verilog. **(10)**
27) Explain Data types in VHDL. **(10)**

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28) Write the VHDL and Verilog HDL codes for 1-bit full adder using dataflow Description. **(10)**
29) Explain the logical operators in VHDL & Verilog HDL in detail. **(10)**
30) What is the significance of std_logic_1164? Explain with example. **(10)**

Question Bank
Unit – II

NOV-DEC 2008

1) Write the data flow description and derive a minimixed Boolean function of the system that has three 1-bit inputs $a_{(2)}$ $a_{(1)}$ $a_{(0)}$ and one 1- bit output Y the least significant bit is $a_{(0)}$, y is '1' only when ($a_{(2)}$ $a_{(1)}$ $a_{(0)}$) = (1,3,6,7) otherwise Y is '0' . **(10)**

2) Find programming errors and write correct statements. **(10)**

i. Process (2), where Z is output.
ii. Y <= Y * i,
iii. Z := Y * i.
iv. Process (N)
begin
variable Y, i : natural.
v. While (i<N) loop
i := i + 1;
Y := Y * i;
end;

3) Draw flow chart, logic symbol for 2:1 mux. Write behavioural description using IF_ELSE statement. **(10)**

MAY-JUNE 2009

4) Derive a minimized Boolean expression for multiplication of a × b where a and b are 2 bit nos. Write a VHDL code for the same using dataflow description. **(10)**

5) Write a VHDL code for description of a 3 bit binary counter using behavioural statement. The counter uses synchronous active high clear signal. **(10)**

6) Define signals and variables in VHDL. Illustrate an example to show difference between signal assignment and variable assignment statement. **(10)**

APRIL/MAY 2010

7) Write a VHDL code for 3 bit down counter with active low synchronous clear in behavioral style of description. **(10)**

8) Design and write a VHDL programming errors in dataflow & behavioral style of description. **(10)**

9) Design & write VHDL code for D latch **(10)**

NOV/DEC 2010

10) Explain the following with ref to VHDL:
i) Signal declaration and assignment statement.
ii) Variable declaration and assignment statement. **(10)**

11)Write VHDL code 0f 2×2 magnitude comparator in data flow style description. **(10)**

12) List common VHDL programming errors in data flow and behavioral style description **(10)**

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13) Write VHDL code for 3-bit carry look ahead adder in data flow style. **(10)**
14) Write code of 4 bit up counter with synchronous active high clear in behavioral style. **(10)**
15) Write code for D-latch using variable assignment statement in behavioral style. **(10)**

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16) Design two bit magnitude comparator of input a_0, a_1, b_0, b_1 and output equal, eless, egreat using dataflow description. **(10)**
17) Write VHDL code for 3 bit counter with active low clear using behavioral Description **(10)**
18) Explain any two sequential statements using example. **(10)**

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19) Design a 2×2 combinational array multiplier and write a dataflow description for the same . **(10)**
20) Explain constants ,signal and variables in VHDL .Give suitable example to illustrate difference between signal and variable . **(10)**
21) Write a behavioral code for 4 bit up decade counter with synchronous active high clear signal. **(10)**

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22) Write a dataflow description in VHDL of a fulladder with enable .If the enable is low(0),the sum and carry are zero;otherwise ,the sum and carry are the usual output of the adder .Use a 7-ns delay for any gate including XOR gate .Draw the truth table and derive the Boolean function after minimization. **(10)**
23) Write the VHDL code for 3 –bit carry look ahead adder in dataflow description. **(10)**
24) Write VHDL code for J-K flip flop using case statement and for D-flipflop using if statement. **(10)**

APRIL /MAY 2013

25) Write VHDL code of 2×2 magnitude comparator in data flow style of description. **(10)**
26) Write VHDL code of 4-bit counter with Asynchronous low clear in behavioral style. **(10)**
27) Explain signal declaration and assignment statement with example. **(10)**

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28) Explain the procedure and function statements with suitable example. **(10)**
29) Give the syntax rule for If statements and case statements and design JK flip flop using above statements. **(10)**
30) Design 4-bit binary to gray code converter using data flow description. **(10)**

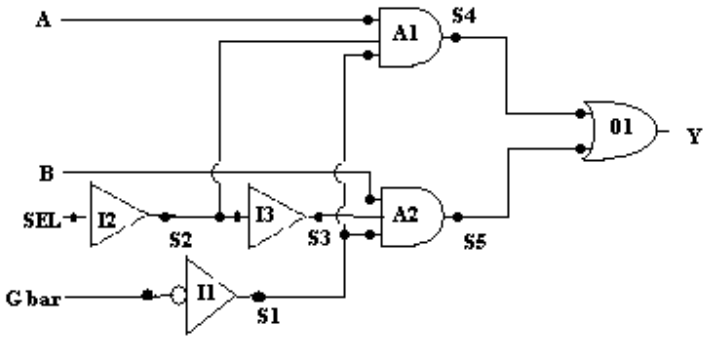
Question Bank
Unit – III

NOV-DEC 2008

1) Design a 3 bit synchronous counter using JK flip flop and write the structural description. **(10)**
2) Derive the switch level logic for NOR with truth table and write switch level description. **(10)**
3) Explain CMOS switch and write code for it. **(10)**

MAY-JUNE 2009

4) Write a structural description for given logic diagram. **(10)**



5) Write a switch level description for a 2 input CMOS NAND gate. **(10)**
6) Explain procedures and functions in VHDL. Give an example to illustrate use of procedure for a full adder using half adder. **(10)**

APRIL/MAY 2010

7) Explain organization of the structural description with example. **(10)**
8) Explain the following with example(any three).
   i) Binding between Entity & Architecture
   ii) Binding between Library &module
   iii) Binding between library & component
   iv) Binding between Entity & component **(10)**
9) Write VHDL behavioral code for MOS switch
   i) NMOS
   ii) PMOS **(10)**

NOV/DEC 2010

10) Draw switch level logic for X-NOR gate with minimum number of transistors and write switch level description for the same. **(10)**
11) Write VHDL code for decade Counter with terminal count using D-Flip Flop **(10)**
12) Write behavioral code for: i) NMOS and ii) PMOS **(10)**

APRIL /MAY 2011

13) Derive switch level logic for 2×1 multiplexer with active high enable and write code for same . **(10)**
14) Explain C-MOS switch and write code for it. **(10)**
15) Write structural description of (N+1) bit magnitude comparator using generate statement. **(10)**

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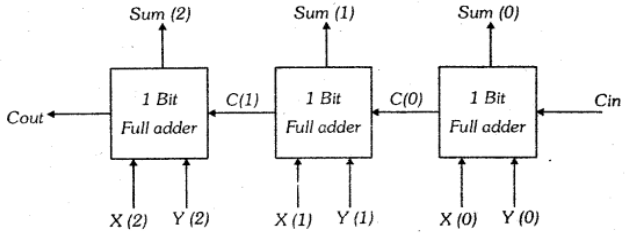
16) Write structural description for full adder. **(10)**
17) Draw and explain serial and parallel combination of switch. **(10)**
18) Write switch level description of AND & OR logic gate. **(10)**

APRIL /MAY 2012

19) Write a structural description for the following 3 bit ripple carry adder .The design should describe the 1 bit full adder used as component. **(10)**



20) What are features of switch level description .List the relationship between source . , drain and gate of NMOS switch and write a VHDL Description for the same. **(10)**
21) Explain generate and generic statements in VHDL .Explain importance of procedure and functions in VHDL. **(10)**

NOVEMBER/DECEMBER 2012

22) Explain Bindings in VHDL with suitable examples. **(10)**
23) Derive the switch level logic for NAND gate with truth table and write switch level description. **(10)**
24) Write a VHDL code for fulladder using Half adder in structural style of description. **(10)**

APRIL /MAY 2013

25) Explain following with example.
i) Binding between Entity and Architecture.
ii) Binding between Library and Component. **(10)**
26)Draw switch level logic for X-NOR gate with minimum number of transistors and write switch level description for the same. **(10)**
27) Design a 2-bit synchronous counter using JK flip-flop and write the structural description. **(10)**

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28) Make the VHDL codes for 4-bit full adder using 1-bit full adders with structural Description. **(10)**
29) Design XOR gate using Switch level description. **(10)**
30) Enlist the advantages of CMOS and design its VHDL module using switch level description. **(10)**

Question Bank
Unit – IV

NOV-DEC 2008

1) What is package? How it allows the user to access built-in constructs? Write code for the package in codes and it has members add, mul, divide and null. **(10)**
2) What is record type? Explain with program that outputs the current temperatures and forecast condition "Sunny". **(10)**
3) Write mixed type description of ALU for given operations. **(10)**

Operation code (OPC)	Operation
00	addition
01	Multiplication
10	division
11	null

MAY-JUNE 2009

4) What is mixed type description? Explain strategy to use mixed type description. Write a mixed type description for 2:1 decoder. **(10)**
5) Explain following in brief referring to file processing in VHDL. **(10)**
   i. File – Open
   ii. File – Close
   iii. Readline
   iv. Write
6) Explain package in detail. Give the statements for declaration and accessing package using an example. **(10)**

APRIL/MAY 2010

7) Design 1 bit full adder & write mixed type description **(10)**
8) Write VHDL code for finding the greatest element of an array for N + 1 element **(10)**
9) Explain file processing with an example. **(10)**

NOV/DEC 2010

10) Write VHDL code for addition of two [5×5] matrices. **(10)**
11) Explain how you will read a file consisting of ASCII character in VHDL. **(10)**
12) Write a VHDL code to find the smallest number among N+1 elements of an array **(10)**

APRIL /MAY 2011

13) Write code for 16×8 SRAM. **(10)**
14) Write code, explain reading a text file containing real numbers **(10)**
15) Write code for finding a greatest element of an array for N+ 1 element. **(10)**

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16) Write VHDL package for package 'codes' whose members are add ,mul , divide, none.Explain why we used package. **(10)**

17) Write mixed type description of an arithmetic logic unit operation selection of ALU. **(10)**

Operation code	Operation
00	addition
01	Multiplication
10	division
11	null

18) Explain different record type with their formats **(10)**

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19) What is mixed type description .Explain strategy to use mixed type description .Write a mixed type description for 2:1 multiplexer and mention styles of descriptions used. **(10)**

20) Explain the following with reference t file processing in V HDL.
i) Readline ii) Writeline
iii) Read iv) Write

21) Explain arrays in VHDL .Write a VHDL description to find greatest number in array A of 5 elements.The array is as follows.
A= ["1100", "1110", " 1010", " 0011", "1101"]. **(10)**

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22) Explain file processing with an example. **(10)**

23) What is record type? Explain with program that outputs the current temperatures and forecast condition. **(10)**

24) Write VHDL description for addition of two [5× 5] matrices. **(10)**

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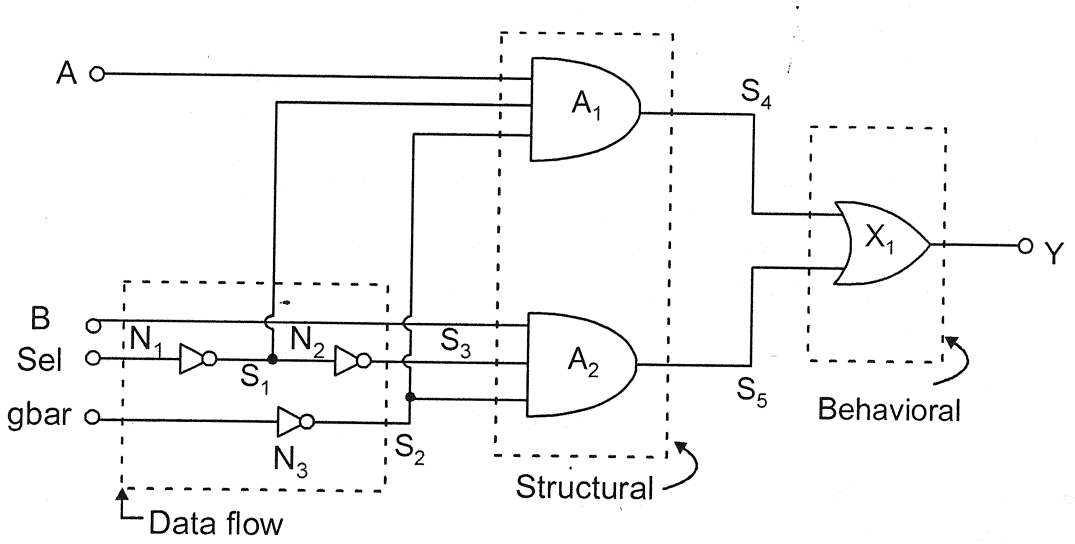
25) What are user defined data types? Give its format and explain with example. **(10)**

26) Write VHDL code for addition of two two [5× 5] matrices. **(10)**

27) Write VHDL code for finding the gratest element of an array of (N+1) elements. **(10)**

NOVEMBER/DECEMBER 2013

28) Write the VHDL codes for following circuit using mixed type description as per mention type in fig. **(10)**



29)What is record type .Explain with example. **(10)**

30)Write the VHDL codes for writing the integer to text using file processing. **(10)**

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Question Bank
Unit – V

NOV-DEC 2008

1) Draw and explain Xilinx Spartan 4000 series FPGA architecture. **(10)**
2) Explain Built in self test. **(10)**
3) How digital pattern generator and logic analyzer have advantages over simulator? Explain. **(10)**

MAY-JUNE 2009

4) Draw and explain architecture of Xilinx 9500 CPLD series. **(10)**
5) What is advantage of debugging tools over simulation tools? Justify with example of digital pattern generator and logic analyzer. **(10)**
6) Explain need of testing logic circuit and various faults occurring in circuit. Discuss various ways of testing circuit. **(10)**

APRIL/MAY 2010

7) Explain with neat diagram architecture of Xilinx Spartan 4000 series FPGA. **(10)**
8) Explain:
   i) Design for testability
   ii) Scan path technique **(10)**
9) Explain fault module for testing logic circuits w.r.t
   i) Stuck at model
   ii) Single & multiple fault
   iii) CMOS circuit. **(10)**

NOV/DEC 2010

10) Explain with neat diagram architecture of Xilinx 9500 series CPLD. **(10)**
11) Write short note on:
   i) Design of testability
   ii) Boundary Scan test. **(10)**
12) Explain logic analyzer with built in digital pattern generator and its advantages over Simulator **(10)**

APRIL /MAY 2011

13) Explain architecture of Xilinx Spartan 4000 series FPGA architecture. **(10)**
14) Write short note on digital pattern generator and logic analyzer. **(10)**
15) Explain path sensitizing and random test. **(10)**

NOVEMBER/DECEMEBR 2011

16) Compare CPLD & FPGA. **(10)**
17) Explain fault module for testing logic circuits. **(10)**
18) Explain the term Advantage of Logic analyzer with built in digital pattern generator over simulator. **(10)**

APRIL /MAY 2012

19) Explain BIST in detail for testing of logic circuits. **(10)**
20) Explain architecture of Xilinx 9500 CPLD series. **(10)**
21) Explain usage of logic analyzer and pattern generator in testing and debugging. **(10)**

NOVEMBER/DECEMBER 2012

22) Draw and explain Xilinx Spartan 4000 series FPGA. **(10)**
23) Explain advantages of logic analyzer with built in pattern generator over simulator. **(10)**
24) Explain
i) Design for testability
ii) Scan path techniques . **(10)**

APRIL /MAY 2013

25) Explain
i) Design for testability
ii) Scan path techniques . **(10)**
26) Compare CPLD & FPGA. **(10)**
27) Explain fault module for testing logic circuits. **(10)**

NOVEMBER/DECEMBER 2013

28) Write Short notes on Stuck at Fault. **(10)**
29) Write Short notes on Boundary Scan test. **(10)**
30) Write Short notes on logic analyzer. **(10)**