SHRI SANT GADGE BABA COLLEGE OF ENGINEERING & TECHONOLOGY, BHUSAWAL
Department of Electronics & Telecommunication Engineering.

Question Bank

Subject: VLSI DESIGN **B.E E&TC (CGPA)**

UNIT- I

MARCH 2016

1. Explain digital design for logic circuit with flowchart. **8**
2. Explain VHDL data types in detail. **8**
3. If A & B are two unsigned variable with A = 1100 & B = 1001 then find the following. **8**
i) A OR B ii) A NOR B
iii) A SLR 3 iv) B ROR 3
v) A & B vi) A AND B
vii) A SLL1 viii) A XNOR B

October 2015

4. State Moore's law and its impact on technology. Explain various types of chips used for design of digital logic systems. **8**
5. Draw a diagram for a typical CAD system. Explain the terms synthesis and simulation with reference to CAD Tools. **8**
6. Explain various operators used in VHDL. **8**

UNIT- II

MARCH 2016

1. Write VHDL code for 1 bit full adder using structural & behavioral style of description **8**
2. VHDL code for BCD to seven segment decoder using selective signal assignment. **8**
3. Explain constants, signals & variables in VHDL. Give suitable example to illustrate difference between signal & variable. **8**

October 2015

4. Explain data flow and behavioral style of description in brief with suitable example of each style. **8**
5. Explain execution of signal assignment statement with suitable example. **8**
6. Explain any two conditional signal assignment statements used in dataflow modeling. **8**

UNIT- III

MARCH 2016

1.	Explain the procedure & function statements with suitable example	**8**
2.	Write VHDL code for 4 bit full adder using structural style of description	**8**
3.	Write VHDL code for JK flip-flop using behavioral style of description.	**8**

October 2015

4.	Explain the features of structural style of design. Explain with suitable example organization of structural design.	**8**
5.	Explain sequential CASE statement in VHDL with a suitable example.	**8**
6.	What is binding in VHDL. State various types of binding in VHDL. Explain any two types with example.	**8**

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UNIT- IV

MARCH 2016

1.	Write VHDL code for CMOS inverter using switch level description.	**8**
2.	Write VHDL code for SR latch using switch level description.	**8**
3.	Write VHDL description for addition of two [4x4] matrices.	**8**

October 2015

4.	Draw switch-level logic diagram for a 2 input NAND gate and write VHDL code for it.	**8**
5.	Draw a switch level logic diagram for a CMOS switch. What are main characteristics of a CMOS Switch? Write a VHDL switch level description for the CMOS switch.	**8**
6.	Explain importance of mixed type description in VHDL over pure dataflow, behavioral or structural descriptions. Explain concept, syntax and importance of package in VHDL.	**8**

UNIT- V

MARCH 2016

1.	Explain the following with reference to file processing in VHDL. i) Readline ii) Read iii) Writeline iv) Write	**8**
2.	Explain stuck at fault model in detail.	**8**
3.	Explain Built in self Test.	**8**

October 2015

4.	Draw and explain structure of a CPLD device.	**8**
5.	Explain any four VHDL procedures for file handling.	**8**
6.	Explain the fault model used in digital circuit.	**8**