SHRI SANT GADGE BABA COLLEGE OF ENGINEERING & TECHONOLOGY, BHUSAWAL
Department of Electronics & Communication Engineering.

B.E E&C -Division (A)

Assignment 1:

1) If A & B are two unsigned variables, with A = 1001 and B = 1111, find the values of following expressions.
   i. (A and B)
   ii. (A ^ B)
   iii. !(B)
   iv. As/r3
   v. (A&&B)

2) Compare between VHDL and Verilog.
3) Write a VHDL description for a Full adder using behavioral and Structural style of modeling.

4) Write the data flow description and derive a minimized Boolean function of the system that has three 1-bit inputs a(2) a(1) a(0) and one 1- bit output Y the least significant bit is a(0), y is '1' only when (a(2) a(1) a(0)) = (1,3,4,5,7) other wise Y is '0'.
5) Draw flow chart, logic symbol for 2:1 mux. Write behavioural description using IF_ELSE statement.

Assignment 2:

1) Derive a minimized Boolean expression for multiplication of a × b where a and b are 2 bit nos. Write a VHDL code for the same using dataflow description.
2) Write a VHDL code for description of a 4 bit binary counter using behavioral statement. The counter uses synchronous active high clear signal.
3) Find programming errors and write correct statements. **(10)**
   i. Process (2), where Z is output.
   ii. Y <= Y * i,
   iii. Z := Y * i.
   iv. Process (N)
   begin
   variable Y, i : natural.
   v. While (i<N) loop
   i := i + 1;
   Y := Y * i;
   end;
4) Design & write VHDL code for D latch
5) Write a VHDL code for 3 bit down counter with active low synchronous clear in behavioral style of description.

Assignment 3:

1) Design a 3 bit synchronous counter using JK flip flop and write the structural description.
2) Derive the switch level logic for NOR with truth table and write switch level description.
3) Write a switch level description for a 2 input CMOS NAND gate.
4) Draw and explain Xilinx Spartan 4000 series FPGA architecture.
5) Draw and explain architecture of Xilinx 9500 CPLD series.