Seat Number

* 6 7 0 3 *

ELECTIVE - I
VLSI Design
(187141 / 237141)

P. Pages : 2

Time : Three Hours **Max. Marks : 80**

Instructions to Candidates :

1. Do not write anything on question paper except Seat No.
2. Graph or diagram should be drawn with the black ink pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.
4. Assume data wherever necessary.

UNIT – I

1. Solve **any two.**

a) Explain digital design for logic circuit with flowchart. **8**

b) Explain VHDL data types in detail. **8**

c) If A & B are two unsigned variable with A = 1100 & B = 1001 then find the following. **8**

i) A OR B
ii) A NOR B
iii) A SLR 3
iv) B ROR 3
v) A & B
vi) A AND B
vii) A SLL1
viii) A XNOR B

UNIT – II

2. Solve **any two.**

a) Write VHDL code for 1 bit full adder using structural & behavioral style of description. **8**

b) Write VHDL code for BCD to seven segment decoder using selective signal assignment. **8**

c) Explain constants, signals & variables in VHDL. Give suitable example to illustrate difference between signal & variable. **8**

UNIT – III

3. Solve **any two.**

a) Explain the procedure & function statements with suitable example. **8**

b) Write VHDL code for 4 bit full adder using structural style of description. **8**

c) Write VHDL code for JK flip-flop using behavioral style of description. **8**

UNIT – IV

4. Solve **any two.**

a) Write VHDL code for CMOS inverter using switch level description. **8**

b) Write VHDL code for SR latch using switch level description. **8**

c) Write VHDL description for addition of two [4x4] matrices. **8**

UNIT – V

5. Solve **any two.**

a) Explain the following with reference to file processing in VHDL. **8**

i) Readline ii) Read
iii) Writeline iv) Write

b) Explain stuck at fault model in detail. **8**

c) Explain Built in self Test. **8**

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