Seat Number

* 2 4 6 0 *

ELECTIVE I
VLSI Design
(187141 / 237141)

P. Pages : 2

Time : Three Hours **Max. Marks : 80**

Instructions to Candidates :

1. Do not write anything on question paper except Seat No.
2. Graph or diagram should be drawn with the black ink pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.
4. All questions are compulsory and carry equal marks.
5. Figures to right indicate full marks.
6. Assume suitable data wherever necessary.
7. Solve **any two** from each question.

UNIT – I

1. Attempt **any two.**

a) State Moore's law and its impact on technology. Explain various types of chips used for design of digital logic systems. **16**

b) Draw a diagram for a typical CAD system. Explain the terms synthesis and simulation with reference to CAD Tools.

c) Explain various operators used in VHDL.

UNIT – II

2. Attempt **any two.** **16**

a) Explain data flow and behavioral style of description in brief with suitable example of each style.

b) Explain execution of signal assignment statement with suitable example.

c) Explain any two conditional signal assignment statements used in dataflow modeling.

UNIT – III

3. Attempt **any two.** **16**

a) Explain the features of structural style of design. Explain with suitable example organization of structural design.

b) Explain sequential CASE statement in VHDL with a suitable example.

c) What is binding in VHDL. State various types of binding in VHDL. Explain any two types with example.

UNIT – IV

4. Attempt **any two.** **16**

a) Draw switch-level logic diagram for a 2 input NAND gate and write VHDL code for it.

b) Draw a switch level logic diagram for a CMOS switch. What is main characteristics of a CMOS Switch? Write a VHDL switch level description for the CMOS switch.

c) Explain importance of mixed type description in VHDL over pure dataflow, behavioral or structural descriptions.
Explain concept, syntax and importance of package in VHDL.

UNIT – V

5. Attempt **any two.** **16**

a) Draw and explain structure of a CPLD device.

b) Explain any four VHDL procedures for file handling.

c) Explain the fault model used in digital circuit.

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